

Quadrics Interconnect Roadmap ISC 2006 Dresden

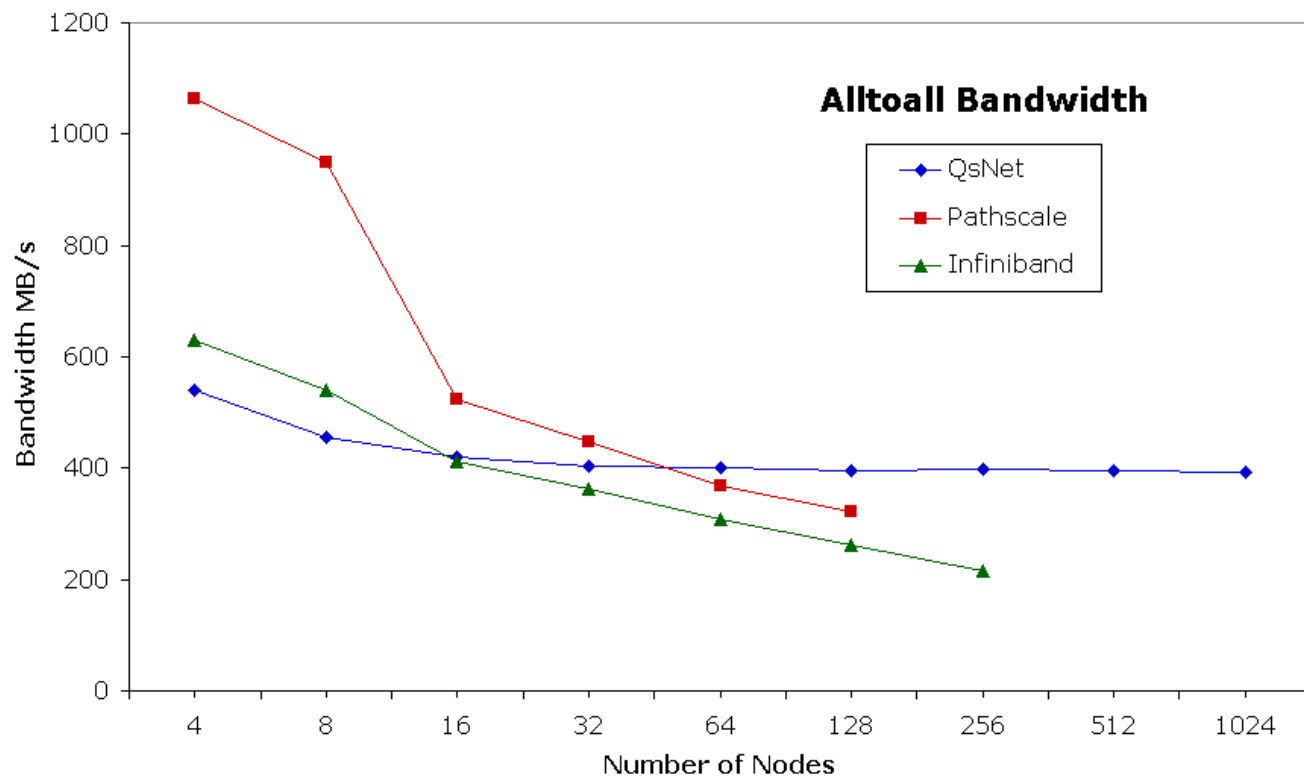
Quadrics Background

- Subsidiary of the Finmeccanica, the Italian Defence and Aerospace group
- Our products:
 - Interconnect
 - Software & support
 - Systems
- 10th anniversary in 2006

QsNet^{II} – Product Highlights

- Industry leading latencies
 - MPI latency 1.2 μs
 - Shmem put latency 0.85 μs
- Scalable bandwidth
 - Adaptive routing
- Optimised collectives
 - Hardware barrier, broadcast
 - Reduction in the NIC

QsNet^{II} – Delivering Scalable Bandwidth



QsNet^{II} Product Highlights

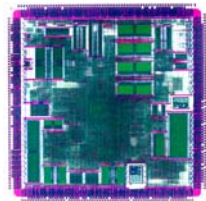
- Continuing to deliver production systems:
 - Tera10, 3 rails × 600 ports
 - First 2048 port QsNet^{II} network
 - Sharcnet – 800 ports



Quadrics Interconnect Strategy

- Combine the economics of commodity and the performance of QsNet.
- Leverage industry standard components to deliver world class HPC products.
- Hardware, software and support from one company.

Implementation Strategy



Single adapter ASIC

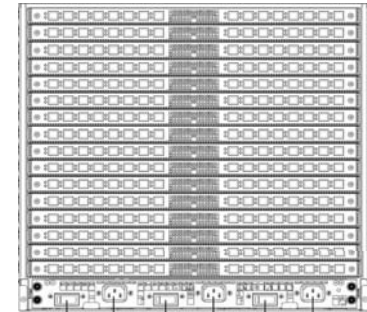


Range of adapters for different markets

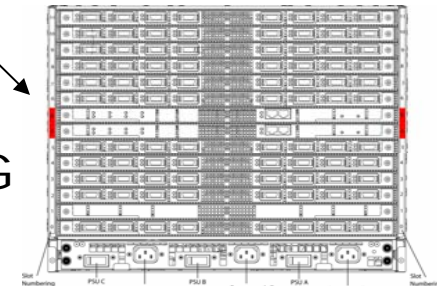


Standard cables, connectors and optics

QsNetIII



QsTenG



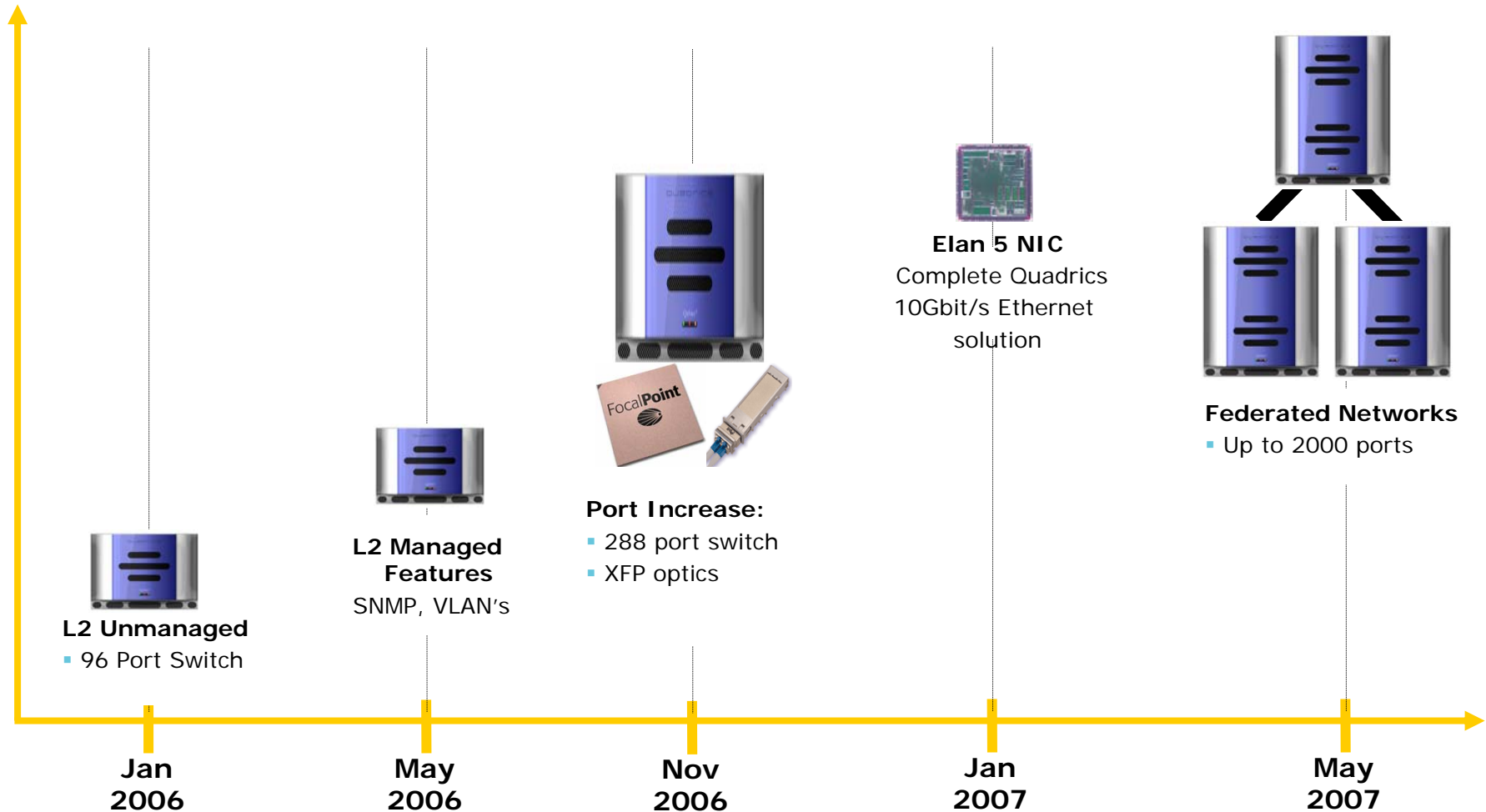
Common switch infrastructure and management software stack

Step 1 – Quadrics Ethernet Switch, QsTenG

- A new generation of 10 Gbit/s Ethernet switch for new classes of bandwidth hungry applications.
- Takes Quadrics scalable switch design into the standards based interconnect market.



QsTenG – 2006/7 Roadmap



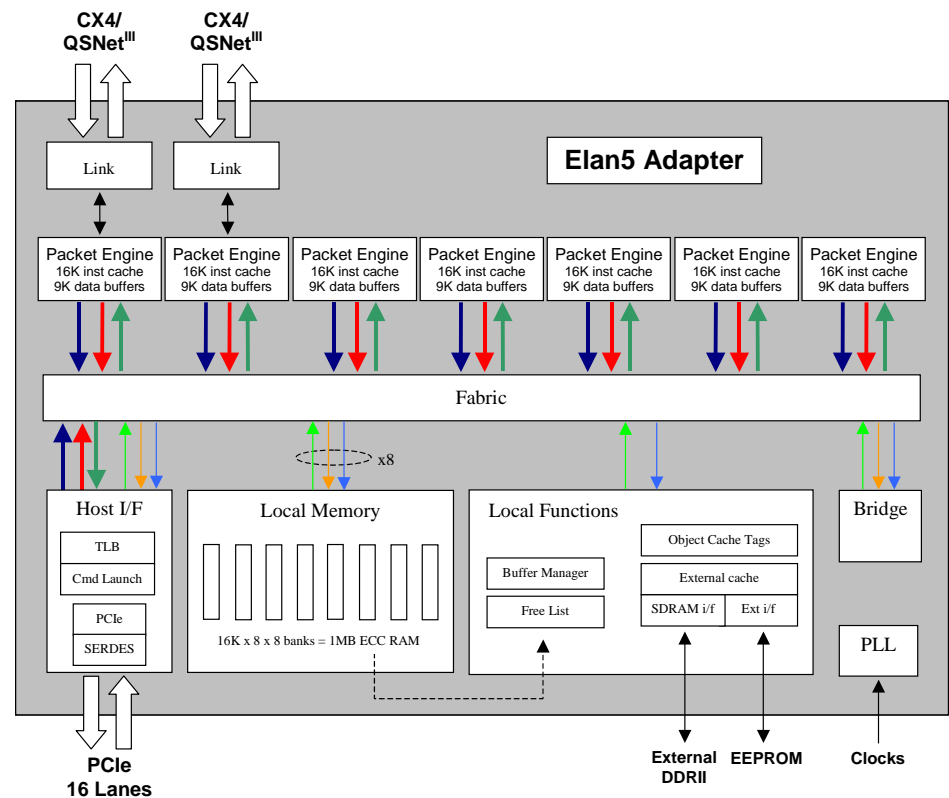
Step 2 – QsNet^{III} Next Generation HPC Network

- New host adapter – Elan5
 - Multiple protocols: Ethernet & QsNet
 - PCI Express 8x, 16x
 - DDR CX4 links

- Custom fabric – Elite5
 - High radix switches
 - HPC specifics: broadcast, barrier, adaptive routing

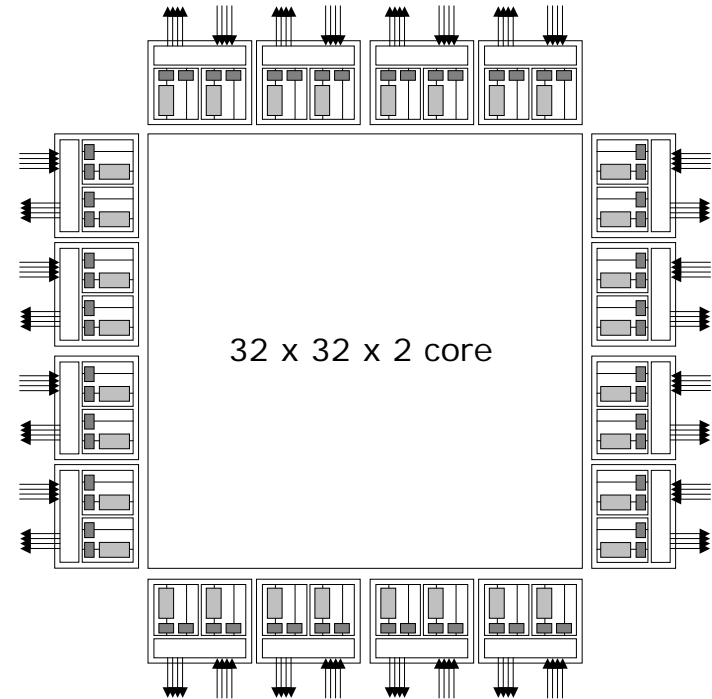
Elan5 – Overview

- 2 × QsNet^{III} or Ethernet link
- Packet Processing Engines
- Local memory system
 - 1MB on chip buffer space, routes, page tables
 - 256MB – 4GB (optional) on the adapter card.
- Memory Management
 - 4 pages sizes 4M-32G
 - TLB (64 × 16 pages)
- Host Interface
 - PCI-Express 16x
 - DDR support

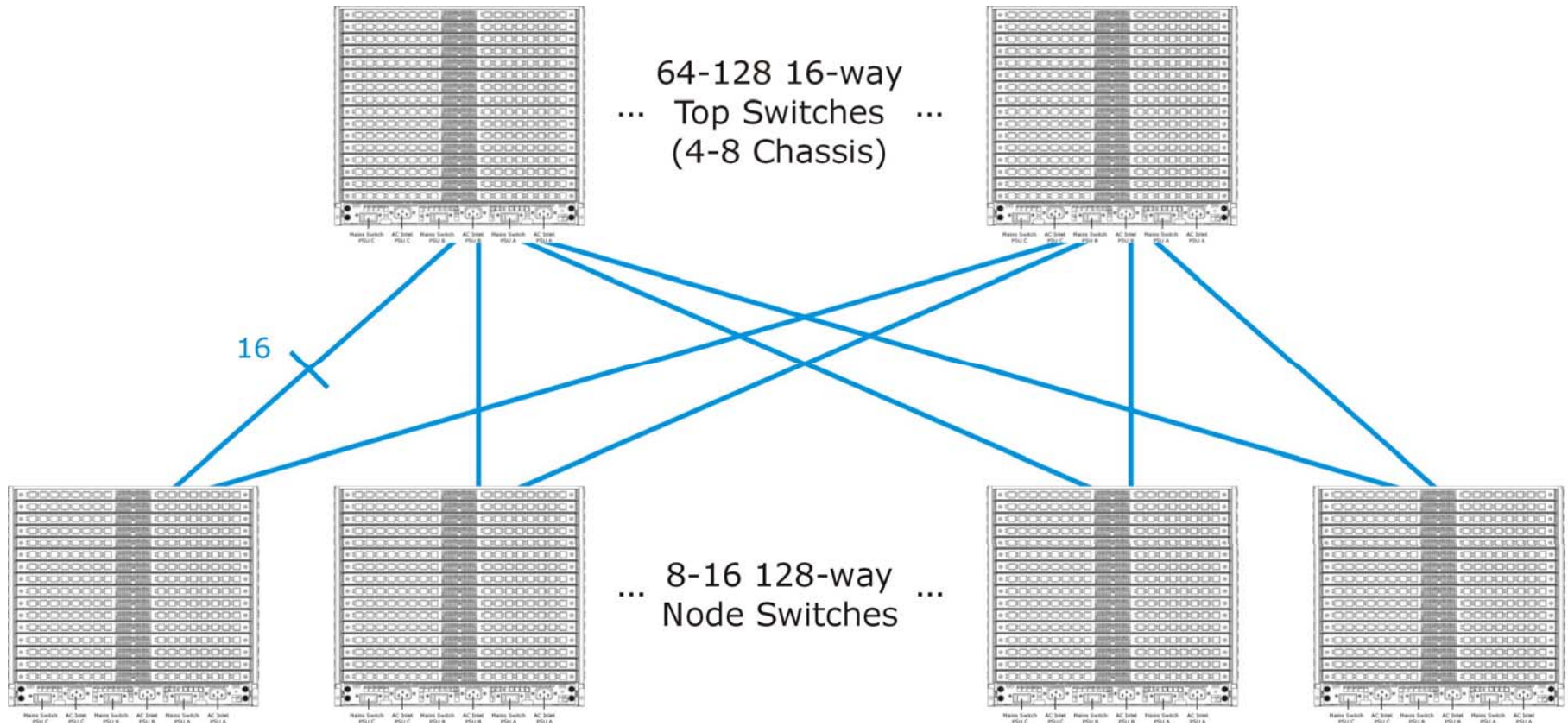


QsNet^{III} Fabric – Elite5

- Physical layer DDR XAUI
 - 4 x 6.25Gbit/s (2.5Gbytes/s) in each direction
- Adaptive routing
- Broadcast & barrier support
- 32 virtual channels per link
- Fat tree or mesh topologies
- 16x4, 32x2 switch component
 - Or multiple x8, x4, x2, x1 switches



1024-2048 Port QsNet^{III} Network



Quadrics Interconnects Compared

	QsNet^I	QsTenG	QsNet^{III}
Protocol	Quadrics proprietary	10GB Ethernet	Quadrics proprietary
Physical layer	10 bits @ 1.333GHz	CX4 4 bits @ 3.125Gb/s	DDR CX4 4 bits @ 6.25Gb/s
Unidirectional rate	920 Mbytes/s	1000 Mbytes/s	2000 Mbytes/s
Bidirectional rate	900 Mbytes/s	1000 Mbytes/s	4000 Mbytes/s
Switch arity	8	12	16/32
Switch hop latency	20ns	450ns	40ns
NIC	Elan4	Commodity or Elan5-10G RDMA	Elan5 - QsNet ^{III}
Bus Interface	PCI-X	PCI-X or PCI Express	16x PCI Express
MPI Latency	1.3uS	~10uS	~1.3uS

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